DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3-6, and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Yu '218. Yu discloses a transistor device comprising: a semiconductor region having a top surface; a source region (22, fig. 1) in the semiconductor region; a drain region (24, fig. 1) in the semiconductor region; a channel region in the semiconductor region between the source region and the drain region and having a top surface proximate the top surface of the semiconductor region; an implanted impurity region (35, fig. 1) within and surrounded (35 is an oxide island, lines 5-12, col. 5) by the channel region and spaced from the top surface, the impurity region having a first outer boundary that is proximate, but laterally spaced apart from the source region and a second outer boundary proximate, but laterally spaced apart from the drain region (fig. 1); a gate (36, fig. 1) overlying the channel region; and a gate dielectric (34, fig. 1) between the gate and the channel region. The semiconductor region comprises a silicon substrate (fig. 1). The source and drain regions extend into the semiconductor region a first distance, and wherein the implanted impurity region is spaced from the top surface by a distance less than the first distance (fig. 1). The gate dielectric comprises silicon dioxide (lines 25-35, col. 5). The implanted impurity region comprises a region of an implanted

oxygen bearing species in the channel region (fig. 1). A first sidewall spacer (32, fig. 1) adjacent a first sidewall of the gate; a second sidewall spacer (32, fig. 1) adjacent a second sidewall of the gate; a lightly doped drain region within the semiconductor region adjacent the drain region (lines 60-65, col. 4), the lightly doped drain region disposed beneath the first sidewall; and a lightly doped source region (lines 60-65, col. 4) within the semiconductor region adjacent the source region, the lightly doped source region disposed beneath the second sidewall.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 7, 9, 10, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu ‘218 in view of Murota ‘289.

a. Yu discloses the device of claim 1 and that the transistor device can be either a PMOS or NMOS (col. 6). Yu, however, does not expressly disclose that the semiconductor region comprises a region of monocrystalline silicon, the channel region comprises a strained channel region, and/or the device may have a CMOS implementation.

b. Murota discloses a transistor device wherein the semiconductor region comprises a region of monocrystalline silicon [0031], the channel region

comprises a strained channel region [0028], and/or the device may have a CMOS implementation [0034].

c. It would have been obvious to one of ordinary skill in the art to have strained the channel, made the semiconductor region out of monocrystalline silicon, and used a CMOS implementation in Yu's device in order to increase device speed and allow for Yu's invention in various applications (e.g. CMOS inverters, etc.).

5. Claims 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu '218.

a. Yu discloses the device of claim 1 and at least a second transistor (inherent as the transitor is comprised in a integrated circuit comprising numerous transistors. Yu however does not expressly disclose that the second transistor to not comprise an impurity region below the gate dielectric.

b. Nevertheless it would have been obvious to one of ordinary skill in the art at the time of the invention to have had the second transistor to not comprise an impurity region below the gate dielectric. since it has been held that omission of an element and its function is obvious if the function of the element is not desired *In re Kuhle*, 526 F.2d 553, 188 USPQ 7 (CCPA 1975). In the instant case this would be to allow for the elimination of the BOX oxide and reference 35 which is effective in reducing sub-threshold leakage but decreases device speed in logic

application MOS transistors of the IC while retaining said element in power application MOS transistors of the IC.

6. Claims 30-37 rejected under 35 U.S.C. 103(a) as being unpatentable over Yu '218 in view of Murota '289.

a. Yu discloses a transistor device and that the transistor device can be either a PMOS or NMOS (col. 6). Yu, however, does not expressly disclose that the semiconductor region comprises a region of monocrystalline silicon, the channel region comprises a strained channel region, and/or the device may have a CMOS implementation.

b. Murota discloses a transistor device wherein the semiconductor region comprises a region of monocrystalline silicon [0031], the channel region comprises a strained channel region [0028], and/or the device may have a CMOS implementation [0034].

c. It would have been obvious to one of ordinary skill in the art to have strained the channel, made the semiconductor region out of monocrystalline silicon, and used a CMOS implementation in Yu's device in order to increase device speed and allow for Yu's invention in various applications (e.g. CMOS inverters, etc.).

PLEASE NOTE: With this modification Yu/Murota disclose a CMOS device, [references cited herein are to Yu] the CMOS device having a P channel and an N channel transistor (fig. 1), comprising: a semiconductor region having a top surface; a first well

doped to an N type formed within the semiconductor region and having a top surface proximate the top surface of the semiconductor region (fig. 1), for the P channel transistor; a P type source region (22, fig. 1) formed in the first well; a P type drain region (24, fig. 1) formed in the first well; a channel region formed in the first well in the semiconductor region between the source region and the drain region and having a top surface proximate the top surface of the semiconductor region; a first implanted impurity region (35, fig. 1) within and surrounded (35 is an oxide island, lines 5-12, col. 5) by the channel region in the first well and spaced from the top surface, the impurity region having a first outer boundary that is proximate, but laterally spaced apart from the source region in the first well and a second outer boundary proximate, but laterally spaced apart from the drain region in the first well (fig. 1); a gate (36, fig. 1) for the P channel transistor overlying the channel region in the first well; a gate dielectric (34, fig. 1) between the gate for the P channel transistor and the channel region in the first well; a second well doped to a P type formed within the semiconductor region and having a top surface proximate the top surface of the semiconductor region (fig. 1), for the N channel transistor; an N type source region formed in the second well; an N type drain region formed in the second well (fig. 1); a channel region formed in the second well in the semiconductor region between the source region and the drain region and having a top surface proximate the top surface of the semiconductor region (fig. 1); a gate for the N channel transistor overlying the channel region in the second well; and a gate dielectric between the gate for the N channel transistor and the channel region in the second well (fig. 1). A second implanted impurity region within and surrounded by the

channel region in the second well and spaced from the top surface, the second implanted impurity region having a first outer boundary proximate, but laterally spaced apart from the source region in the second well and a second outer boundary that is proximate, but laterally spaced apart from the drain region in the second well (fig. 1). The semiconductor region comprises a silicon substrate. The first implanted impurity region comprises a region of an implanted oxygen bearing species in the channel region (fig. 1).

Response to Arguments

Applicant's arguments filed 7-21-08 have been fully considered but they are not persuasive.

d. Applicant argues that a CVD process is used instead of oxygen implantation which would yield an implanted oxygen bearing species. Examiner notes, however that These limitations invoke the Product-by-Process doctrine. Product-by-process limitations are not limited by the manipulations of the recited steps, only the structure implied by the steps (MPEP 2113). Specifically the fact that the impurity region is implanted does not appear to structurally distinguish the invention over the resulting structure produced by the prior art. The burden to show that the claimed method **necessarily** distinguishes over the prior art is on the applicant.

e. Applicant's remaining arguments have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AMAR MOVVA whose telephone number is (571)272-9009. The examiner can normally be reached on 7:30 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly Nguyen can be reached on 571-272-2402. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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